

Remarks

The non-final Office Action dated December 28, 2009 indicates that claims 13-20 have been withdrawn from consideration after restriction. The following rejections are presented: claims 1-7 stand rejected under 35 U.S.C. § 102(a) over Knoll (U.S. Patent No. 7,205,188); and claims 8-12 stand rejected under 35 U.S.C. § 103(a) over the ‘188 reference in view of AAPA. In the following discussion, Applicant traverses the rejections, and does not acquiesce in any regard to averments in this Office Action (unless Applicant expressly indicates otherwise).

Applicant respectfully traverses the withdrawal of claims 13-20 as the Examiner has failed to meet the requisite burden in making the restriction requirement, which requires a determination in accordance with relevant PCT Articles, as this application is a § 371(c) application in which unity of invention was found at the PCT stage. More specifically, M.P.E.P. § 1850 requires that, “during the national stage as a Designated or Elected Office under 35 U.S.C. 371, PCT Rule 13.1 and 13.2 will be followed when considering unity of invention of claims of different categories.” The relevant framework of the statutes and rules require the USPTO Examiner to make an Agency determination that there is a lack of Unity of Invention, according to the PCT Articles, Rules (13) and Administrative instructions including Annex B (*see* M.P.E.P. § 1850, citing *Caterpillar Tractor Co. v. Commissioner of Patents and Trademarks*, 650 F. Supp. 218, 231 USPQ 590 (E.D. Va. 1986)). Applicant thus maintains its request for withdrawal of the restriction requirement. Furthermore, as claims 13-20 do not stand rejected, Applicant requests allowance of the claims.

Applicant respectfully traverses the § 102(a) and § 103(a) rejection of all claims because the cited ‘188 reference either alone or in combination with “AAPA” lacks correspondence to the claimed invention. Referring to the rejection of claim 4 as an example, the cited portions of the ‘188 reference fail to disclose limitations directed to an integrated circuit device having a monocrystalline silicon substrate, and to creating a window in a layer and forming monocrystalline SiGe on an exposed portion of the substrate (as relevant to claim 1, from which claim 4 depends). Referring to cited FIG. 1c of the ‘188 reference, the substrate (0) is referred to as a “Si wafer” with no mention of any monocrystalline silicon. In addition, cited FIG. 1b and items 6/6a/6b do not

disclose a “monocrystalline SiGe layer” in which the SiGe is formed on an exposed substrate; rather, the “SiGe-base layer 6” is actually formed on a “Si-buffer layer 6a,” which is formed after the creation of an opening (see column 4:4-19).

Moreover, it appears that the formation of the SiGe-base layer 6 in accordance with the purpose of the ‘188 reference must be upon the Si-buffer layer 6a, relative to an underlying substrate, thus failing to correspond to limitations directed to the formation of SiGe on an exposed substrate. Referring to column 4:27-33 of the ‘188 reference, “[w]hat is essential for manufacture in accordance with the invention of the SiGe-HBTs is that in the SiGe-layer deposition process the doping profile for the base of the bipolar structures, in the vertical direction, is enclosed by a C-atom profile” Accordingly, the vertical arrangement of the lower Si-buffer layer 6a, mid-level SiGe-base layer 6 and upper Si-cover layer 6b is important to suit this purpose of the ‘188 reference, and cannot correspond to the claimed invention.

Applicant notes that claim 1 has been amended in a manner that is believed to be consistent with the claim as previously presented in view of the specification as filed. Amended claim 1 recites that the created base-window is made in a layer on an underlying substrate, as consistent with all figures and description in the instant application, and that the SiGe layer is formed in the created base-window and upon the exposed underlying substrate. *See*, for example, FIG. 2 and discussion at paragraph 0027 of the published version of the instant application for discussion of related example embodiments. As discussed above, the ‘188 reference requires that a silicon buffer layer (Si-buffer 6a) be formed upon an underlying substrate, with the asserted SiGe layer (base layer 6) formed thereupon. Accordingly, the ‘188 reference fails to disclose limitations in amended claim 1, as well as claims 2-12 which depend therefrom. Applicant therefore believes that the § 102 rejections of claims 1-7, as well as the § 103 rejections of claims 8-12 (which depend from claim 1 and rely upon the same teachings in the ‘188 reference), lack correspondence and requests that the rejections be removed.

Applicant further traverses the § 103 rejection of claims 8-12 because the cited references teach away from the Office Action’s proposed combination. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main reference - the rationale being

that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007) (“when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.”). Applicant submits that the combination would render the invention inoperable because, as consistent with the cited portions of the instant application, the use of SiGe with varactor diodes “severely degrades the current gain of a pnp bipolar transistor, rendering it virtually unusable in this application” (see page 1:20-23 of the instant application). This is consistent with page 2:1-2 of Applicant’s specification, which goes on to state that “[h]ence, the known methods approach for integrating the LPNP and VCAP [varactor diode] cannot be directly used in SiGe BiCMOS.” Nothing in the Office Action or in the asserted art addresses these issues, as the cited ‘188 reference fails to recognize and disclose any manner in which to overcome the same. Under M.P.E.P. § 2143.01, the rejections cannot be maintained.

As consistent with the above discussion regarding the explicit teaching away in the asserted “AAPA” (Applicant’s disclosure), Applicant further submits that there is no motivation to modify the ‘188 reference as asserted. Specifically, the alleged motivation relies upon the cited portion of Applicant’s disclosure (which teaches away from the combination). The Office Action goes on to acknowledge that the cited ‘188 reference “is silent in using lateral pnp transistor, varactor diode and a polysilicon resistor” as in Applicant’s disclosure. Nothing in the cited art indicates any rationale for solving the problems as presented in Applicant’s disclosure, including those relating to the integration of LPNP and VCAP devices with SiGe substrates. It thus appears that the Office Action has used Applicant’s specification and claims in an improper hindsight-based attempt to modify the primary ‘188 reference and arrive at the claimed invention. The Office Action has therefore failed to provide a valid reason, from the prior art, for making the proposed combination, contrary to the requirements of Section 103 and relevant law. *See, e.g., KSR* at 1741 (“A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art.”). Similarly, “rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” (*In re Kahn*, 441 F. 3d 977, 988 (CA Fed. 2006) cited with approval in *KSR*). As the Office Action has

provided no rationale from the prior art that supports the proposed combination of references, there is no motivation to make the combination and the § 103 rejection should be removed.

In view of the above, Applicant believes that each of the rejections is improper and should be withdrawn and that the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Juergen Krause-Polstorff, of NXP Corporation at (408) 408-9062 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By:



Robert J. Crawford
Reg. No.: 32,122
Eric J. Curtin
Reg. No.: 47,511
651-686-6633
(NXPS.671PA)